

74AHC157; 74AHCT157

Quad 2-input multiplexer

Rev. 02 — 9 November 2007

Product data sheet

1. General description

The 74AHC/AHCT157 are high-speed Si-gate CMOS devices and are pin compatible with Low Power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74AHC/AHCT157 are quad 2-input multiplexer which select 4 bits of data from two sources under the control of a common data select input (S). The enable input (\bar{E}) is active LOW. When \bar{E} is HIGH, all of the outputs (1Y to 4Y) are forced LOW regardless of all other input conditions.

Moving the data from two groups of registers to four common output buses is a common use of the 74AHC/AHCT157. The state of the common data select input (S) determines the particular register from which the data comes. It can also be used as function generator. The device is useful for implementing highly irregular logic by generating any four of the 16 different functions of two variables with one variable common. The 74AHC/AHCT157 is logic implementation of a 4-pole, 2-position switch, where the position of the switch is determined by the logic levels applied to S.

The logic equations are:

$$1Y = \bar{E} \times (1I1 \times S + 1I0 \times \bar{S})$$

$$2Y = \bar{E} \times (2I1 \times S + 2I0 \times \bar{S})$$

$$3Y = \bar{E} \times (3I1 \times S + 3I0 \times \bar{S})$$

$$4Y = \bar{E} \times (4I1 \times S + 4I0 \times \bar{S})$$

The 74AHC/AHCT157 is identical to the 74AHC/AHCT158 but has non-inverting (true) outputs.

2. Features

- Balanced propagation delays
- All inputs have a Schmitt-trigger action
- Inputs accept voltages higher than V_{CC}
- Multiple input enable for easy expansion
- Ideal for memory chip select decoding
- For 74AHC157 only: operates with CMOS input levels
- For 74AHCT157 only: operates with TTL input levels
- ESD protection:
 - ◆ HBM JESD22-A114E exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
 - ◆ CDM JESD22-C101C exceeds 1000 V

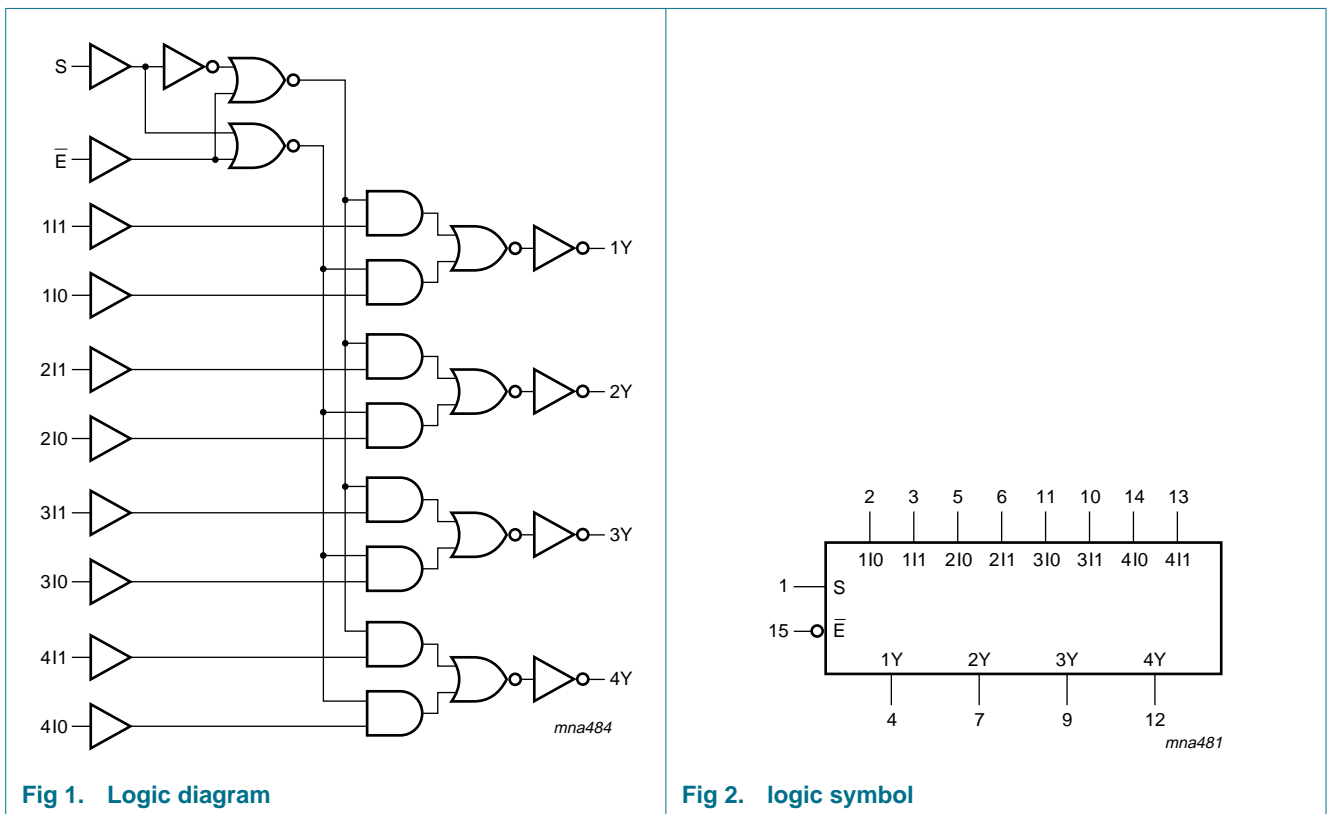
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

| Type number | Package | | | Version |
|---------------------------|-------------------|----------|--|----------|
| | Temperature range | Name | Description | |
| 74AHC157D 74AHCT157D | -40 °C to +125 °C | SO16 | plastic small outline package; 16 leads; body width 3.9 mm | SOT109-1 |
| 74AHC157PW 74AHCT157PW | -40 °C to +125 °C | TSSOP16 | plastic thin shrink small outline package; 16 leads; body width 4.4 mm | SOT403-1 |
| 74AHC157BQ 74AHCT157BQ | -40 °C to +125 °C | DHVQFN16 | plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm | SOT763-1 |

4. Functional diagram



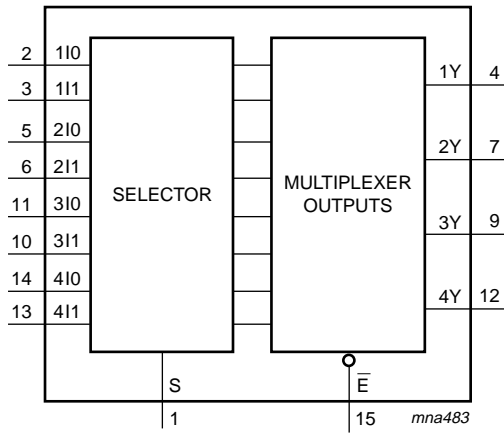


Fig 3. Logic symbol

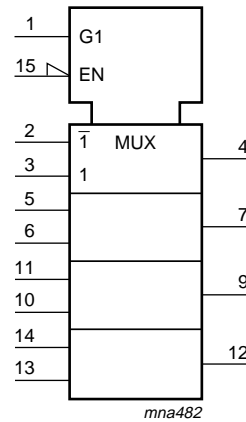


Fig 4. IEC logic symbol

5. Pinning information

5.1 Pinning

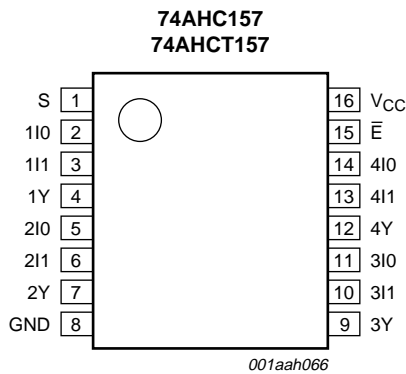
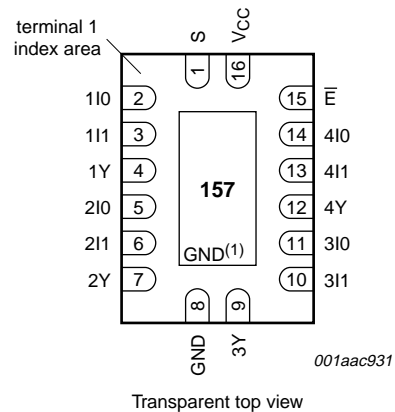


Fig 5. Pin configuration SO16, TSSOP16



- (1) The die substrate is attached to this pad using conductive die attach material. It can not be used as a supply pin or input.

Fig 6. Pin configuration DHVQFN16

5.2 Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|-----------------|--------------|---------------------------|
| S | 1 | common data select input |
| 1I0 to 4I0 | 2, 5, 11, 14 | data inputs from source 0 |
| 1I1 to 4I1 | 3, 6, 10, 13 | data inputs from source 1 |
| 1Y to 4Y | 4, 7, 9, 12 | multiplexer outputs |
| GND | 8 | ground (0 V) |
| \bar{E} | 15 | enable input (active LOW) |
| V _{CC} | 16 | supply voltage |

6. Functional description

Table 3. Function table^[1]

| Input | | | | Output |
|-----------|---|-----|-----|--------|
| \bar{E} | S | nI0 | nI1 | nY |
| H | X | X | X | L |
| L | L | L | X | L |
| L | L | H | X | H |
| L | H | X | L | L |
| L | H | X | H | H |

[1] H = HIGH voltage level;
 L = LOW voltage level;
 X = don't care.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|-------------------------|--|---------|------|------|
| V_{CC} | supply voltage | | -0.5 | +7.0 | V |
| V_I | input voltage | | -0.5 | +7.0 | V |
| I_{IK} | input clamping current | $V_I < -0.5$ V | [1] -20 | - | mA |
| I_{OK} | output clamping current | $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V | [1] - | ±20 | mA |
| I_O | output current | $V_O = -0.5$ V to $(V_{CC} + 0.5$ V) | - | ±25 | mA |
| I_{CC} | supply current | | - | 75 | mA |
| I_{GND} | ground current | | -75 | - | mA |
| T_{stg} | storage temperature | | -65 | +150 | °C |
| P_{tot} | total power dissipation | $T_{amb} = -40$ °C to +125 °C | | | |
| | SO16 package | | [2] - | 500 | mW |
| | TSSOP16 package | | [3] - | 500 | mW |
| | DHVQFN16 package | | [4] - | 500 | mW |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] P_{tot} derates linearly with 8 mW/K above 70 °C.

[3] P_{tot} derates linearly with 5.5 mW/K above 60 °C.

[4] P_{tot} derates linearly with 4.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | 74AHC157 | | | 74AHCT157 | | | Unit |
|---------------------|-------------------------------------|--------------------------|----------|-----|----------|-----------|-----|----------|------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| V_{CC} | supply voltage | | 2.0 | 5.0 | 5.5 | 4.5 | 5.0 | 5.5 | V |
| V_I | input voltage | | 0 | - | 5.5 | 0 | - | 5.5 | V |
| V_O | output voltage | | 0 | - | V_{CC} | 0 | - | V_{CC} | V |
| T_{amb} | ambient temperature | | -40 | +25 | +125 | -40 | +25 | +125 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC} = 3.3$ V ± 0.3 V | - | - | 100 | - | - | - | ns/V |
| | | $V_{CC} = 5.0$ V ± 0.5 V | - | - | 20 | - | - | 20 | ns/V |

9. Static characteristics

Table 6. Static characteristics

Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|---|---------------------------|--|-------|-----|------|------------------|------|-------------------|------|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| For type 74AHC157 | | | | | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 2.0 V | 1.5 | - | - | 1.5 | - | 1.5 | - | V |
| | | V _{CC} = 3.0 V | 2.1 | - | - | 2.1 | - | 2.1 | - | V |
| | | V _{CC} = 5.5 V | 3.85 | - | - | 3.85 | - | 3.85 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 2.0 V | - | - | 0.5 | - | 0.5 | - | 0.5 | V |
| | | V _{CC} = 3.0 V | - | - | 0.9 | - | 0.9 | - | 0.9 | V |
| | | V _{CC} = 5.5 V | - | - | 1.65 | - | 1.65 | - | 1.65 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | | | |
| | | I _O = -50 μA; V _{CC} = 2.0 V | 1.9 | 2.0 | - | 1.9 | - | 1.9 | - | V |
| | | I _O = -50 μA; V _{CC} = 3.0 V | 2.9 | 3.0 | - | 2.9 | - | 2.9 | - | V |
| | | I _O = -50 μA; V _{CC} = 4.5 V | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | I _O = -4.0 mA; V _{CC} = 3.0 V | 2.58 | - | - | 2.48 | - | 2.40 | - | V |
| I _O = -8.0 mA; V _{CC} = 4.5 V | 3.94 | - | - | 3.8 | - | 3.70 | - | V | | |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | | | |
| | | I _O = 50 μA; V _{CC} = 2.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 50 μA; V _{CC} = 3.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 50 μA; V _{CC} = 4.5 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 4.0 mA; V _{CC} = 3.0 V | - | - | 0.36 | - | 0.44 | - | 0.55 | V |
| I _O = 8.0 mA; V _{CC} = 4.5 V | - | - | 0.36 | - | 0.44 | - | 0.55 | V | | |
| I _I | input leakage current | V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V | - | - | 0.1 | - | 1.0 | - | 2.0 | μA |
| I _{CC} | supply current | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V | - | - | 4.0 | - | 40 | - | 80 | μA |
| C _I | input capacitance | | - | 3.0 | 10 | - | 10 | - | 10 | pF |
| C _O | output capacitance | | - | 4.0 | - | - | - | - | - | pF |
| For type 74AHCT157 | | | | | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 4.5 V to 5.5 V | 2.0 | - | - | 2.0 | - | 2.0 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 4.5 V to 5.5 V | - | - | 0.8 | - | 0.8 | - | 0.8 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V | | | | | | | | |
| | | I _O = -50 μA | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | I _O = -8.0 mA | 3.94 | - | - | 3.8 | - | 3.70 | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V | | | | | | | | |
| | | I _O = 50 μA | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 8.0 mA | - | - | 0.36 | - | 0.44 | - | 0.55 | V |

Table 6. Static characteristics ...continued
 Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|-----------------|---------------------------|---|-------|-----|------|------------------|-----|-------------------|-----|---------------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| I_I | input leakage current | $V_I = 5.5\text{ V or GND};$ $V_{CC} = 0\text{ V to }5.5\text{ V}$ | - | - | 0.1 | - | 1.0 | - | 2.0 | μA |
| I_{CC} | supply current | $V_I = V_{CC}\text{ or GND}; I_O = 0\text{ A};$ $V_{CC} = 5.5\text{ V}$ | - | - | 4.0 | - | 40 | - | 80 | μA |
| ΔI_{CC} | additional supply current | per input pin; $V_I = V_{CC} - 2.1\text{ V}; I_O = 0\text{ A};$ other pins at V_{CC} or GND; $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | - | - | 1.35 | - | 1.5 | - | 1.5 | mA |
| C_I | input capacitance | | - | 3 | 10 | - | 10 | - | 10 | pF |
| C_O | output capacitance | | - | 4.0 | - | - | - | - | - | pF |

10. Dynamic characteristics

Table 7. Dynamic characteristics
 GND = 0 V; For test circuit see [Figure 9](#).

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|--------|-----------|------------|-------|--------------------|-----|------------------|-----|-------------------|-----|------|
| | | | Min | Typ ^[1] | Max | Min | Max | Min | Max | |

For type 74AHC157

| | | | | | | | | | | |
|---|-------------------|--|------|-----|------|-----|------|-------------|------|-------------|
| t_{pd} | propagation delay | $nI0, nI1\text{ to }nY;$ see Figure 7 ^[2] | | | | | | | | |
| | | $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ | | | | | | | | |
| | | $C_L = 15\text{ pF}$ | - | 4.4 | 9.7 | 1.0 | 11.5 | 1.0 | 12.5 | ns |
| | | $C_L = 50\text{ pF}$ | - | 6.3 | 13.2 | 1.0 | 15.0 | 1.0 | 16.5 | ns |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | | | | | | | | |
| | | $C_L = 15\text{ pF}$ | - | 3.2 | 6.4 | 1.0 | 7.5 | 1.0 | 8.0 | ns |
| | | $C_L = 50\text{ pF}$ | - | 4.6 | 8.4 | 1.0 | 9.5 | 1.0 | 10.5 | ns |
| | | $S\text{ to }nY;$ see Figure 7 ^[2] | | | | | | | | |
| | | $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ | | | | | | | | |
| | | $C_L = 15\text{ pF}$ | - | 4.8 | 13.6 | 1.0 | 16.0 | 1.0 | 17.0 | ns |
| | | $C_L = 50\text{ pF}$ | - | 6.8 | 17.1 | 1.0 | 19.5 | 1.0 | 21.5 | ns |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | | | | | | | | |
| | | $C_L = 15\text{ pF}$ | - | 3.6 | 8.6 | 1.0 | 10.0 | 1.0 | 11.0 | ns |
| | | $C_L = 50\text{ pF}$ | - | 5.2 | 10.6 | 1.0 | 12.0 | 1.0 | 13.5 | ns |
| | | $\bar{E}\text{ to }nY;$ see Figure 8 ^[2] | | | | | | | | |
| | | $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ | | | | | | | | |
| $C_L = 15\text{ pF}$ | - | 5.9 | 13.2 | 1.0 | 15.5 | 1.0 | 16.5 | ns | | |
| $C_L = 50\text{ pF}$ | - | 8.4 | 16.7 | 1.0 | 19.0 | 1.0 | 21.0 | ns | | |
| $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | | | | | | | | | | |
| $C_L = 15\text{ pF}$ | - | 4.2 | 8.1 | 1.0 | 9.5 | 1.0 | 10.5 | ns | | |
| $C_L = 50\text{ pF}$ | - | 6.0 | 10.1 | 1.0 | 11.5 | 1.0 | 13.0 | ns | | |

Table 7. Dynamic characteristics ...continued
GND = 0 V; For test circuit see Figure 9.

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|---------------------------|-------------------------------|--|-------|--------------------|------|------------------|------|-------------------|------|------|
| | | | Min | Typ ^[1] | Max | Min | Max | Min | Max | |
| C _{PD} | power dissipation capacitance | C _L = 50 pF; f _i = 1 MHz; V _I = GND to V _{CC} ^[3] | | | | | | | | |
| | | 4 outputs switching via S | - | 31 | - | - | - | - | - | pF |
| | | 1 outputs switching via I | - | 13 | - | - | - | - | - | pF |
| For type 74AHCT157 | | | | | | | | | | |
| t _{pd} | propagation delay | nI0, nI1 to nY; see Figure 7 ^[2] | | | | | | | | |
| | | V _{CC} = 4.5 V to 5.5 V | | | | | | | | |
| | | C _L = 15 pF | - | 3.2 | 6.4 | 1.0 | 7.5 | 1.0 | 8.0 | ns |
| | | C _L = 50 pF | - | 4.6 | 8.7 | 1.0 | 9.8 | 1.0 | 11.0 | ns |
| | | S to nY; see Figure 7 | | | | | | | | |
| | | V _{CC} = 4.5 V to 5.5 V | | | | | | | | |
| | | C _L = 15 pF | - | 3.7 | 8.6 | 1.0 | 10.0 | 1.0 | 11.0 | ns |
| | | C _L = 50 pF | - | 5.2 | 10.4 | 1.0 | 12.0 | 1.0 | 13.0 | ns |
| | | \bar{E} to nY; see Figure 8 ^[2] | | | | | | | | |
| | | V _{CC} = 4.5 V to 5.5 V | | | | | | | | |
| | | C _L = 15 pF | - | 4.7 | 8.1 | 1.0 | 9.5 | 1.0 | 10.5 | ns |
| | | C _L = 50 pF | - | 6.7 | 10.6 | 1.0 | 12.0 | 1.0 | 13.5 | ns |
| C _{PD} | power dissipation capacitance | C _L = 50 pF; f _i = 1 MHz; V _I = GND to V _{CC} ^[3] | | | | | | | | |
| | | 4 outputs switching via S | - | 41 | - | - | - | - | - | pF |
| | | 1 outputs switching via I | - | 16 | - | - | - | - | - | pF |

[1] Typical values are measured at nominal supply voltage (V_{CC} = 3.3 V and V_{CC} = 5.0 V).

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] C_{PD} is used to determine the dynamic power dissipation P_D (μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

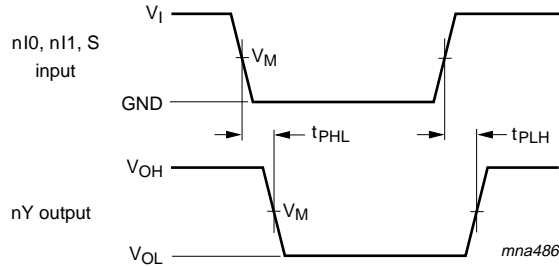
f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in Volts.

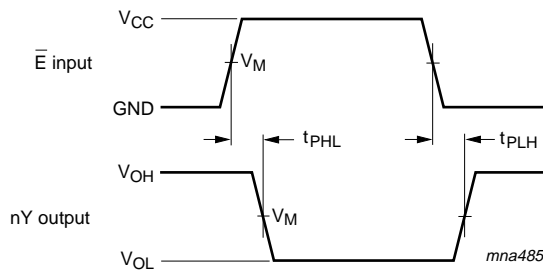
11. Waveforms



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 7. Propagation delay input (nI0, nI1, S) to output (nYn)



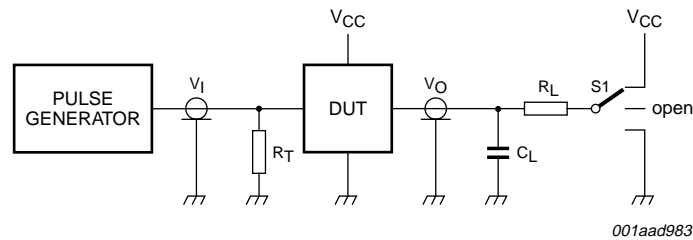
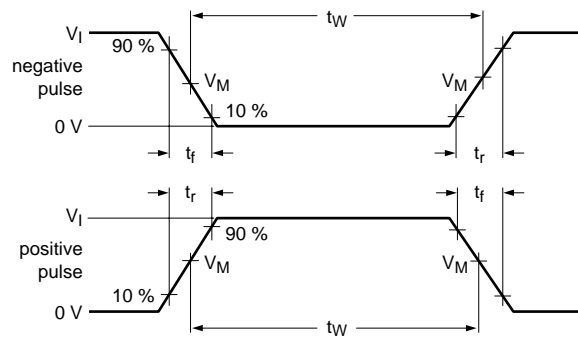
Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 8. Propagation delay input (\bar{E}) to output (nY)

Table 8. Measurement points

| Type | Input | Output |
|-----------|-------------|-------------|
| | V_M | V_M |
| 74AHC157 | $0.5V_{CC}$ | $0.5V_{CC}$ |
| 74AHCT157 | 1.5 V | $0.5V_{CC}$ |



001aad983

Test data is given in [Table 9](#).

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator

C_L = Load capacitance including jig and probe capacitance

R_L = Load resistor

S1 = Test selection switch

Fig 9. Load circuitry for switching times

Table 9. Test data

| Type | Input | | Load | | S1 position | | |
|-----------|----------|------------|--------------|--------------|--------------------|--------------------|--------------------|
| | V_I | t_r, t_f | C_L | R_L | t_{PHL}, t_{PLH} | t_{PZH}, t_{PHZ} | t_{PZL}, t_{PLZ} |
| 74AHC157 | V_{CC} | 3.0 ns | 15 pF, 50 pF | 1 k Ω | open | GND | V_{CC} |
| 74AHCT157 | 3.0 V | 3.0 ns | 15 pF, 50 pF | 1 k Ω | open | GND | V_{CC} |

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

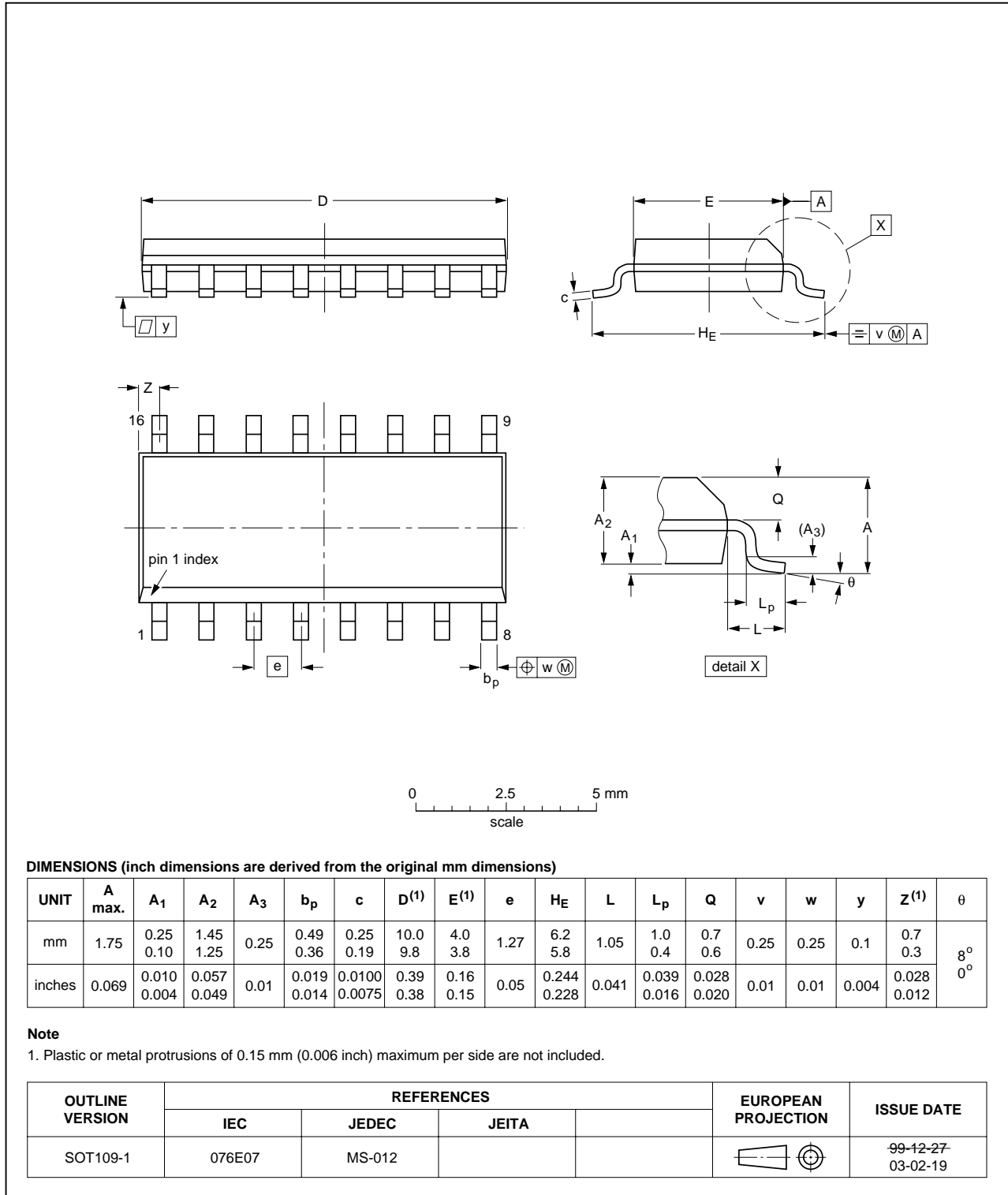


Fig 10. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

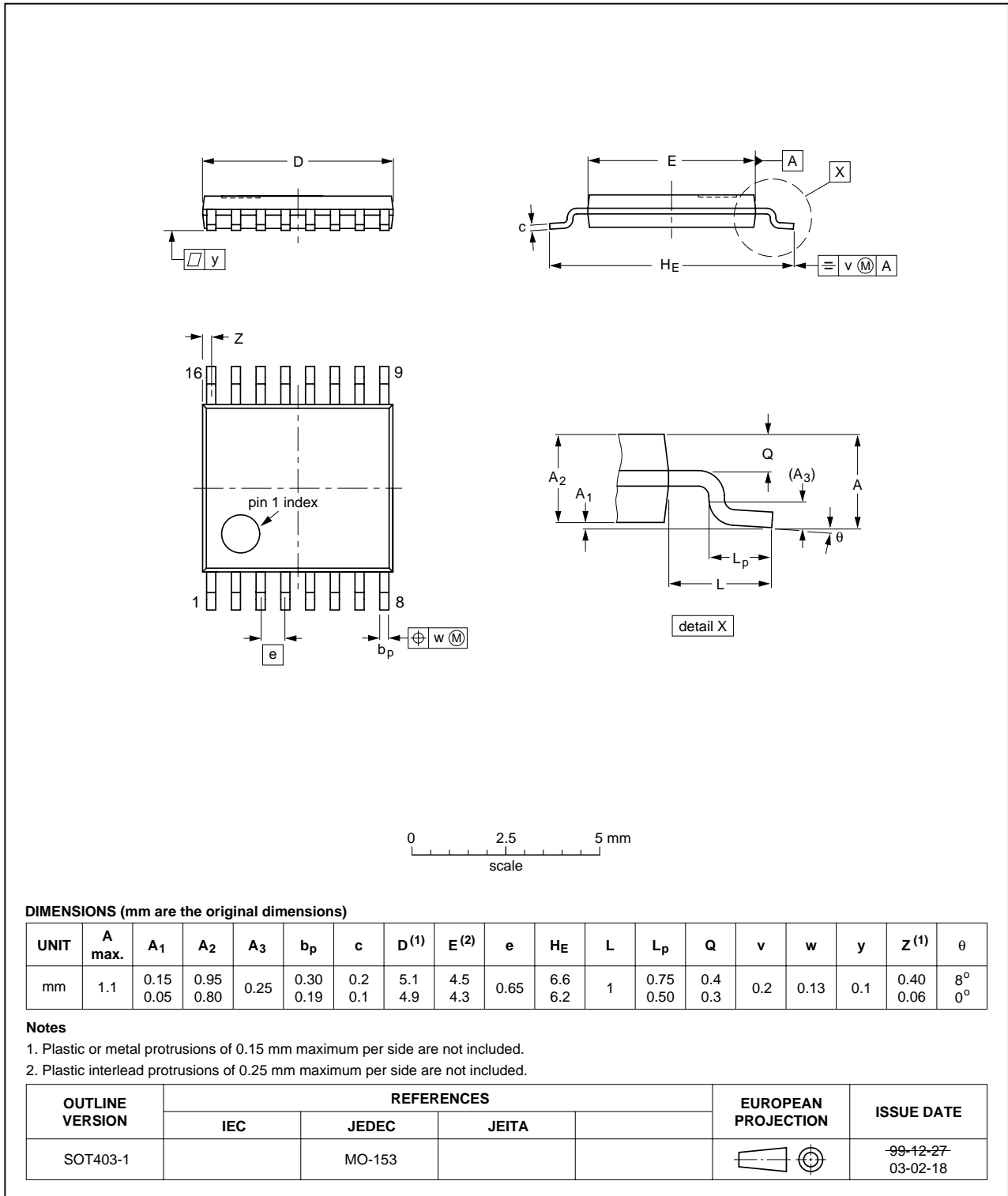


Fig 11. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

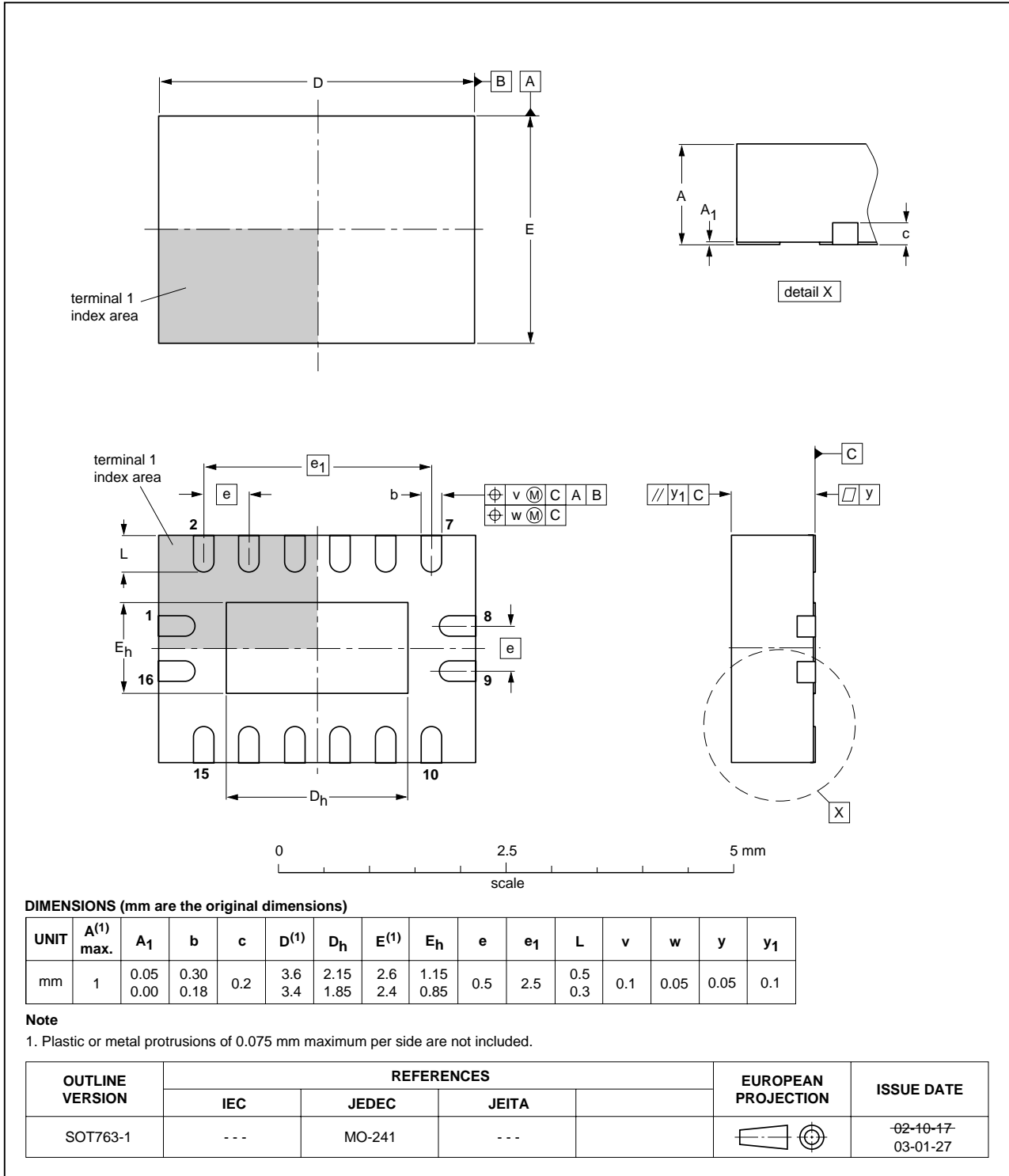


Fig 12. Package outline SOT763-1 (DHVQFN16)

13. Abbreviations

Table 10. Abbreviations

| Acronym | Description |
|---------|---|
| CDM | Charged-Device Model |
| CMOS | Complementary Metal Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

14. Revision history

Table 11. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|-----------------|--|-----------------------|---------------|-----------------|
| 74AHC_AHCT157_2 | 20071109 | Product data sheet | - | 74AHC_AHCT157_1 |
| Modifications: | <ul style="list-style-type: none"> • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Section 3: DHVQFN16 package added. • Section 8: derating values added for DHVQFN16 package. • Section 12: outline drawing added for DHVQFN16 package. | | | |
| 74AHC_AHCT157_1 | 19990924 | Product specification | - | - |

15. Legal information

15.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

15.2 Definitions

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